IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA INC., HYNIX SEMICONDUCTOR U.K. LTD., and HYNIX SEMICONDUCTOR DEUTSCHLAND GmbH, Plaintiffs, v. RAMBUS INC., Defendant.	No. CV-00-20905 RMW ORDER DENYING HYNIX'S MOTION FOR SUMMARY JUDGMENT OF INVALIDITY OF U.S. PATENT NOS. 6,378,020 AND 5,915,105 UNDER 35 U.S.C. §§ 102 AND/OR 103 **[Re Docket No. 763]**

Hynix seeks summary judgment of invalidity based on two prior art references that it contends render claims 32 and 36 of U.S. Patent No. 6,378,020 ("the '020 patent"), and claim 34 of U.S. Patent No. 5,915,105 ("the '105 patent") obvious or anticipated under 35 U.S.C. §§ 102 and 103. Rambus opposes the motion. The court has read the moving and responding papers and considered the arguments of counsel. For the reasons set forth below, the court DENIES Hynix's motion for summary judgment.

I. BACKGROUND

A. U.S. Patent No. 4,330,852 ("Redwine")

The Redwine patent, filed on November 23, 1979 and issued on May 18, 1982, discloses a "Semiconductor Read/Write Memory Array Having Serial Access."

B. U.S. Patent No. 4,922,141 ("Lofgren")

The Lofgren patent, filed on June 3, 1988 and issued on May 1, 1990, discloses a "Phase-Locked Loop Delay Line."

The Patent Examiner considered the Redwine patent during prosecution of the '020 patent, but did not consider Redwine during prosecution of the '105 patent. In addition, the Patent Examiner did not consider Lofgren during prosecution of either the '020 or '105 patents.

C. Invalidity and Obviousness Contentions

Hynix contends that asserted claim 32 of the '020 patent (and claims 30 and 31 upon which claim 32 relies) is anticipated by the Redwine patent and therefore rendered invalid under 35 U.S.C. § 102. In addition, Hynix argues that asserted claim 36 of the '020 patent (and claim 35 upon which claim 36 relies) is obvious in light of the Redwine patent in combination with the Lofgren patent. *See* 35 U.S.C. § 103. Finally, Hynix asserts that claim 34 of the '105 patent is invalid as obvious in light of Redwine in combination with Lofgren.[1] *See id.*

II. ANALYSIS

A. Asserted Claim 32 of the '020 Patent

A person is not entitled to a patent if the invention was patented or described in a printed publication more than one year prior to the date of the application, under Section 102(b), or prior to the date of conception, under Section 102(a). *See* 35 U.S.C. § 102. "To anticipate a claim, a prior art reference must disclose every limitation of the claimed invention, either explicitly or inherently." *Minnesota Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed. Cir. 1992)*; Atlas Powder Co. v. Ireco Inc.*, 190 F.3d 1342 (Fed. Cir. 1999); *Glaxo Inc. v.*

[1]In so arguing, Hynix submits that claim 31 of the '105 patent, upon which claim 34 relies, is anticipated by Redwine.

Novopharm Ltd., 52 F.3d 1043, 1047 (Fed. Cir. 1995). The question of whether a claim limitation is inherent in a prior art reference is a factual issue on which evidence may be introduced. *See Diversitech Corp. v. Century Steps, Inc.*, 850 F.2d 675, 677 (Fed. Cir. 1988); *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991); *In re Graves*, 69 F.3d 1147, 1151 (Fed. Cir. 1995); *In re Schrieber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997). Because anticipation is generally an issue of fact, "[t]he burden of proving invalidity on summary judgment is high[,]" i.e., clear and convincing. *Schumer v. Laboratory Computer Systems, Inc.*, 308 F.3d 1304, 1316 (Fed. Cir. 2002).

In defining the meaning of key terms in a claim, a party may reference the specification, the prosecution history, prior art, and other claims. *See Monsanto*, 948 F.2d at 1268 ("entirely proper" to use specification to determine what inventor meant by terms and phrases in claims). However, it is the claims of the patent that must be anticipated, since the claims define the invention. *See Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988).

1. Independent Claim 30 of the '020 Patent (Integrated Circuit Device Limitation)[2]

Claim 30 recites in part:

> An integrated circuit device comprising:
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> > input receiver circuitry to sample an operation code synchronously with respect to a first transition of an external clock signal, the operation code specifying a read operation; []

Hynix contends that each limitation of claim 30 is anticipated by the Redwine patent.

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[2]Claim 30 in its entirety recites:

> An integrated circuit device comprising:
>
> > input receiver circuitry to sample an operation code synchronously with respect to a first transition of an external clock signal, the operation code specifying a read operation; and
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> output driver circuitry to output data in response to the operation code, wherein:
>
> > the output driver circuitry outputs a first portion of data in response to a rising edge transition of the external clock signal; and
> > the output driver circuitry outputs a second portion of data in response to a falling edge transition of the external clock signal.

Rambus responds, *inter alia*, that the patent examiner specifically considered the Redwine patent during prosecution, so there is a strong inference that the Redwine patent is not Section 102 prior art. *See McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1353 (Fed. Cir. 2001). The parties agree that the Redwine patent discloses "an integrated circuit device." The parties disagree over whether the Redwine patent discloses the remaining limitations of claim 30.

a. External clock signal

"External clock signal" has been construed by this court to mean "a periodic signal from a source external to the device to provide timing information." Claim Construction Order at 30. Hynix argues that the clock generator and control circuitry 30 of the Redwine patent, as represented in block diagram Fig. 1, and the timing diagram of Fig. 2(f)-(h) (a graphic representation of voltage versus time), which references an external clock signal Φ, meet this limitation. Mot. at 8; Redwine Chart at 1.

Rambus counters that the Redwine patent does not contain an external clock signal because it lacks the required "periodic signal." More specifically, in Fig. 2(f) of the Redwine patent, Φ is not periodic. Rambus notes that during both read and write operations there is a time period where Φ is not signaling. *See* Murphy Decl. ¶ 44 (citing Fig. 2(f), annotation above Fig. 2(a)).

Hynix argues in reply that Rambus's reliance on Fig. 2(f) of Redwine, without reference to Figs. 1 and 3, is in error. Hynix submits that Redwine Fig. 1 shows that CS[3] acts as a gate for the external signal Φ, while Redwine Fig. 3, in the upper left hand corner, discloses how the external signal Φ is controlled by CS\ and becomes internal clock signals Φ1 and Φ2. Fig. 2(f), in contrast, depicts a period both before a write operation, when the Φ external clock signal is "gated" by the transistor CS (CS\ stays high), and after CS signals a write operation (when CS\ falls to low). *See* Taylor Decl. Ex. A at 3, 5-6. Hynix submits that regardless of whether CS is low or high, Redwine Figs. 1 and 3, reviewed in combination with Fig. 2, clearly disclose that the external signal Φ continues to run periodically and is continuously applied to the input pin. Taylor Decl. ¶ 8. Hynix further notes that "[i]t would be unnecessary to have the Φ external clock signal gated (internally on

[3]Chip select. *See* Taylor Expert Report re: Invalidity ¶ 9.

the device) by the CS\ signal if the Φ external clock signal was not being continuously received by the device." Taylor Decl. ¶ 8. The court agrees, and finds that Redwine discloses the "external clock signal" limitation.

b. Operation code . . . specifying a read operation

"Operation code" as construed by this court is "one or more bits to specify a type of action." Claim Construction Order at 18. Hynix contends that the "W" signal referenced in Fig. 2 of the Redwine patent specifies either a read or write operation, and therefore meets this limitation. Brown Decl. Ex. D ("Taylor Invalidity Expert Report") Chart 5 ("Redwine Chart") at 2-3. In the specification, Redwine explains:

> For a read operation, the W signal on input 29 is high during the period seen in FIG. 2b, and the data output on the terminal 27 will occur during the time period of 128 cycles seen in FIG. 2d. For a write operation, the W signal must be low as seen in FIG. 2b and the data-in bits must be valid during the preceding time period of 128 cycles seen in FIG. 2e.

Redwine patent at 4:8-14.

Rambus counters that Redwine teaches commands using "transition-based signals" as opposed to bits specifying a read or write action, i.e., Redwine "discloses commands based on the transition of, not the state of, the RAS signal and the W signal held high or low." Murphy Decl. ¶ 45. As support, Rambus notes that the Redwine patent discusses "when RAS goes low," indicating that it teaches commands using transition-based signals. *See id.*

Hynix responds that the W signal when high specifies a read operation, and when low specifies a write operation. *See* Redwine Patent at 4:8-11. Based on the Redwine patent specification, it appears clear that neither the read nor write operations is signaled based on when the W signal is transitioning from one state to another. In addition, even assuming that W was a transition-based signal, W would still constitute a bit specifying a read or write operation. The court finds that the W signal constitutes an operation code.

c. Input receiver circuitry that samples "synchronously with respect to a first transition of an external clock signal"

Hynix submits that the input receiver circuitry of the Redwine patent, Fig. 1 block 30, receives and samples the operation code, here the W signal 29. Hynix relies on the Fig. 2 timing

diagram to establish a known timing relationship between the start of the read cycle when signal W is sampled and the outputting of data in response to external clock Φ. Taylor also opines that one skilled in the art would know that the W and Φ signals are generated in relation to a system clock, and thus have a known timing relationship with each other. Redwine Chart at 3; Mot. at 8 (citing *Helifix*, 208 F.3d at 1339 (limitation need not be disclosed to anticipate if one skilled in the art would understand publication to disclose the element)). Thus, Hynix argues that Redwine discloses input receiver circuitry, block 30, which samples the operation code W signal synchronously with respect to a first transition of the external clock signal Φ.

Rambus argues that the Redwine patent teaches "sensing" the signal "W," as opposed to the '020 patent which would "sample" the signal "W." Murphy Decl. ¶ 46. Apparently, if the W signal were sampled, it would not be held either high or low for the entire operation, as in the timing diagram of Fig. 2. As an example, Rambus notes that an "AND gate" can "sense" the state of a digital signal at a particular point in time without "capturing" the state of that signal. Murphy Decl. ¶ 46. In addition, Rambus notes that block 30 in Fig. 1 does not receive the alleged external clock signal Φ, and there is no disclosure to one of skill in the art of W having a known timing relationship with respect to Φ. Murphy Decl. ¶¶ 46-47.

On reply, Hynix argues that Rambus's distinction between "sensing" and "sampling" is incorrect, and that both terms are interchangeable with "latching," which is the mechanism by which the memory device samples both address information and the W signal. *See* Taylor Reply Decl. ¶ 10. Hynix fails to provide explicit support in the Redwine specification supporting this conclusion. *See Printing Plate Supply Co. v. Crescent Engraving Co.*, 246 F. Supp. 654, 668 (W.D. Mich. 1965) ("It would have been an easy matter to use the same term throughout the application, and since this is not the case, it must be assumed that the use of two different terms indicates that two different meanings are intended."). As such, Hynix's argument is insufficient to establish as a matter of law

that there is no distinction between "sensing," "sampling" and "latching."[4]

In addition, Hynix does not address Rambus's argument that block 30 does not receive the alleged external clock signal Φ, and also fails to address Rambus's assertion that one of skill in the art would not assume that W and Φ have to be generated in relation to a system clock because these signals could be generated independently. *See* Murphy Decl. ¶¶ 46-47. Accordingly, Hynix's argument that the Redwine patent discloses input receiver circuitry that samples "synchronously with respect to a first transition of an external clock signal" as a matter of law is insufficient.

2. Independent Claim 30 of the '020 Patent (Output Circuitry Limitation)

The output circuitry limitation of claim 30 requires:

> output driver circuitry to output data in response to the operation code, wherein:
>
> > the output driver circuitry outputs a first portion of data in response to a rising edge transition of the external clock signal; and
> > the output driver circuitry outputs a second portion of data in response to a falling edge transition of the external clock signal.

Hynix submits that in Redwine, output driver circuitry is included in Fig. 1 block 26, with corresponding details further disclosed in the top center of Fig. 3. Specifically, the NOR gate 75 in Fig. 3 outputs data from the memory device in response to the operation code (which includes the bit value of the W signal), indicating a read operation. Redwine Chart at 3 (citing Fig. 1 block 26, c. 4 l:8-11; c.7 l:47-53, c.3 l:59-63). In turn, Fig. 2 of Redwine shows that the output driver circuitry NOR gate 75 outputs a first portion of data (i.e., 128 of the 256 bits) in response to a rising edge transition of external clock Φ, and a second portion of data (the second 128 bits) in response to a falling edge transition of Φ. *See* Redwine Patent at 3:59-63; Redwine Chart at 3.

Rambus reiterates its argument that Φ is not periodic, as required by the court's construction of external clock signal, and therefore does not meet the external clock signal limitation of claim

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[4] According to a technical dictionary, sampling is "[t]he process of obtaining the values of a function for regularly or irregularly spaced distinct values of an independent variable." IEEE 100: THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS 1001 (7th ed. 2000). A sampling circuit (sampler) is "[a] circuit whose output is a series of discrete values representative of the values of the input at a series of points in time. *Id.* However, a sensing circuit is a circuit whose function is to detect the occurrence of some event at its input terminals. *Id.* at 1025. Finally, a latch is "[a] circuit that can be used to hold data in a ready position until required; usually controlled by another circuit." *Id.* at 608.

30(b). Murphy Decl. ¶ 49 (citing Redwine Patent Fig. 2, annotation above line a). Because Redwine discloses the "external clock signal" limitation, the output circuitry limitation of claim 30 is met.

3. Dependent Claim 31 of the '020 Patent

Claim 31 recites: "The integrated circuit device of claim 30 further including a memory array having a plurality of memory cells." Hynix submits that Fig. 1 of the Redwine patent shows memory sections 10a and 10b, both of which contain 32,768 memory cells. Redwine Patent Fig. 1 c:2, l:55-59; Redwine Chart at 3-4.

Rambus relies on its previous arguments for claim 30, asserting that the Redwine prior art does not disclose an "external clock signal," or specify a timing relationship between /RAS and Φ. Murphy Decl. ¶¶ 50-51. As discussed above, the "external clock signal" limitation is met, but whether input receiver circuitry that samples "synchronously with respect to a first transition of an external clock signal" is disclosed remains a factual question.

4. Underlying Question of Fact on Anticipation of Claim 32 of the '020 Patent

Claim 32 recites: "The integrated circuit device of claim 31 wherein the input receiver circuitry receives address information synchronously with respect to the external clock signal." Hynix argues that Fig. 1 of the Redwine patent shows input receiver circuitry which includes address latches 14, that receive address information via address input lines 16. Hynix submits that the "address latches receive address information synchronously with respect to the RAS signal, because there is a known timing relationship between the time address latches receive and latch the row address and when RAS goes low." Mot. at 9 (citing Redwine Chart at 4). The Redwine Patent states that "[w]hen RAS goes low as seen in Fig. 2a, clocks derived from RAS cause the buffers 14 to accept and latch the eight bits then appearing on the input lines 16." Redwine Patent at 4:4-8. Hynix further argues that – as with the relationship between W and Φ – one skilled in the art would know that RAS and Φ are generated in relation to a system clock, and have a known timing relationship with each other. Redwine Chart at 4.

Rambus argues that – as with the relationship between W and Φ – there is nothing in the

Redwine patent to suggest that RAS and Φ signal are generated in relation to a system clock or that they have a known timing relationship with one another. Murphy Decl. ¶ 52. In addition, Rambus argues that during the period in Redwine Fig. 2 when RAS is asserted, Φ is not toggling, so address information cannot be sampled synchronously with respect to Φ. *See id*; *compare* Redwine Patent Fig. 2(a) *with id.* Fig. 2(f). Murphy also states that one of skill in the art would not know that RAS and Φ are generated in relation to a system clock, or would have a known timing relationship with one another. *See* Murphy Decl. ¶ 52. For the reasons discussed above with regard to claim 30 of the '020 patent, the court finds that a question of fact remains as to whether claim 32 of the '020 patent is anticipated.

B. Asserted Claim 36 of the '020 Patent

Hynix argues that dependent claims 35 and 36 of the '020 patent are obvious in light of the Redwine patent in combination with the Lofgren patent under 35 U.S.C. § 103. As an initial matter, because Hynix has failed to establish that Redwine anticipates claim 30 of the '020 patent, upon which claims 35 and 36 rely, Hynix's argument under section 103 is insufficient as Lofgren is only relevant to the added limitations. The court will nevertheless discuss certain sub-issues.

A patent claim is obvious, and thus invalid, when the differences between the claimed invention and the prior art "are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103; *see also Graham v. John Deere Co.*, 383 U.S. 1, 14 (1966). While obviousness is ultimately a legal determination, it is based on several underlying issues of fact, namely: (1) the scope and content of the prior art; (2) the level of skill of a person of ordinary skill in the art; (3) the differences between the claimed invention and the teachings of the prior art; and (4) the extent of any objective indicia of non-obviousness. *See Graham*, 383 U.S. at 17-18. In addition, "secondary considerations [such] as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented. As indicia of obviousness or nonobviousness, these inquiries may have relevancy." *Graham*, 383 U.S. at 17-18; *see Dann v. Johnston*, 425 U.S. 219, 230 n.4 (1976).

When obviousness is based on the teachings of multiple prior art references, the movant must also establish some "suggestion, teaching, or motivation" that would have led a person of ordinary skill in the art to combine the relevant prior art teachings in the manner claimed. *See Tec Air, Inc. v. Denso Mfg. Mich. Inc.*, 192 F.3d 1353, 1359-60 (Fed. Cir. 1999); *Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc.*, 75 F.3d 1568, 1572 (Fed. Cir. 1996). The nonmovant may rebut a prima facie showing of obviousness with evidence refuting the movant's case or with other objective evidence of nonobviousness. *See WMS Gaming, Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1359 (Fed. Cir.1999). "The reason, suggestion, or motivation to combine [prior art references] may be found explicitly or implicitly: 1) in the prior art references themselves; 2) in the knowledge of those of ordinary skill in the art that certain references, or disclosures in those references, are of special interest or importance in the field; or 3) from the nature of the problem to be solved, 'leading inventors to look to references relating to possible solutions to that problem.'" *Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 665 (Fed. Cir. 2000) (quoting *Pro-Mold*, 75 F.3d at 1572). "In order to prevent a hindsight-based obviousness analysis, we have clearly established that the relevant inquiry for determining the scope and content of the prior art is whether there is a reason, suggestion, or motivation in the prior art or elsewhere that would have led one of ordinary skill in the art to combine the references." *Ruiz*, 234 F.3d at 665. The Federal Circuit has consistently held that a person of ordinary skill in the art must not only have had some motivation to combine the prior art teachings, but some motivation to combine the prior art teachings in the particular manner claimed. *See, e.g., In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000) ("Particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed.").

1. Claim 35 of the '020 Patent

Claim 35 recites: "The integrated circuit device of claim 30 further including a clock alignment circuit to receive the external clock signal." Hynix submits that, to the extent the '020 "clock alignment circuit" can be interpreted to cover a DLL or PLL, the Lofgren patent meets this limitation. Hynix argues that the "external clock signal" is met by Redwine Fig. 1 Φ, as discussed

above. *See* Redwine Patent Figs. 1, 3, c.4, l.59-62,[5] c. 5, l:55-57.

Hynix argues that Lofgren provides an explicit motivation to combine the DLL circuit with a DRAM memory chip:

> The present invention relates to a delay circuit for providing an output signal which is delayed by a precise amount with respect to an input signal. Such circuits are typically referred to as "delay lines" and have many applications. For example, delay lines are commonly used in data separator phase-locked loops used in disc drive systems. *Delay lines are also used to provide optimum timing for control of high speed dynamic RAM devices, which comprise the main memory of virtually all personal computers.*

Brown Decl. Ex. F ("Lofgren UK Patent Application GB 2 197 553 A," hereinafter "Lofgren UK Patent App.") at 1, l:7-18 (emph. added); Taylor Invalidity Report Chart 11 (hereinafter "On-chip DLL/PLL Chart") at 5. Lofgren also notes: "The present invention is especially useful in systems in which a crystal oscillator or other reference timing signal source is already provided in the circuit." Lofgren UK Patent App. at 6, l:37-40.

Hynix argues that DRAM chips exhibit this functionality, as "each chip receives a master external clock signal with which output must be synchronized." Mot. at 11 (citing On-chip DLL/PLL Chart at 5). Based on the Redwine and Lofgren prior art, and the motivation to combine them found in Lofgren, Hynix contends that claim 35 of the '020 patent is obvious and invalid as a matter of law.

Rambus counters that one of ordinary skill in the art would not have been motivated to combine the Redwine and Lofgren prior art references, and that even together they do not meet every limitation of claim 36. *See* Murphy Decl. ¶ 57. First, Rambus concedes that the Lofgren reference discloses a delay-locked loop. *See id*. ¶ 56. Second, Rambus asserts that Lofgren teaches a clock alignment circuit external to the memory chip rather than on the memory chip. *Id.* Third, Rambus contends that the Lofgren application discusses conventional DRAMS based on signal transitions of /RAS and /CAS signals, and therefore does not relate to "synchronous" DRAMs. *Id.* Fourth, Rambus submits expert testimony by Murphy which discusses evidence of a long-felt need

[5] "The register is operated by a two phase clock Φ1, Φ2, plus delayed clocks Φ1d and Φ2d, which are derived from a clock Φ supplied from external to the chip."

for the invention of the '020 patent, and argues that Hynix fails to apply the four factual inquiries required in an obviousness determination. *See* Taylor Expert Report ¶¶ 223-235; Opp. at 12 (citing Murphy Decl. ¶¶ 53-58).

Finally, even though Lofgren disclosed a DLL, Rambus submits that neither the DLL could "lock" onto the signal Φ disclosed in the Redwine patent, as Rambus contends that Φ is not a periodic signal. Murphy Decl. ¶ 57. Thus, Rambus argues that the limited scope and content of the prior art references dictate against an obviousness determination.

On reply, Hynix focuses on the previously cited motivation to combine, and notes that Lofgren discloses a variable delay line. *See* Lofgren Patent at 2:25-35 (". . . thus varying the delay provided by the overall delay line."). As discussed above, independent claim 30 upon which claim 35 relies is not anticipated as a matter of law. In addition, there remains a question of fact as to whether one of ordinary skill would be motivated to combine the Lofgren and Redwine prior art references, or whether Lofgren teaches away from such a combination, e.g., whether Lofgren suggests a clock alignment circuit external to the memory chip, rather than on it. *See* Taylor Decl. ¶ 57; *In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000) (person of ordinary skill in the art must not only have had some motivation to combine prior art teachings, but some motivation to combine prior art teachings in particular manner claimed). The motion for summary judgment of invalidity of claim 35 is denied.

2. Underlying Question of Fact on Obviousness of Claim 36 of the '020 Patent

Claim 36 recites: "The integrated circuit device of claim 35 wherein the clock alignment circuit generates an internal clock signal, and the output driver circuitry outputs data in response to the internal clock signal." Hynix relies on its previous arguments for claim 35 of the '020 patent, asserting that Lofgren discloses a DLL which would receive the external clock signal Φ and generate an internal clock signal. *See, e.g.*, Lofgren UK Patent App. Fig. 2A-B; Redwine Chart at 5. As the argument goes, the "clock alignment circuit" is met by the Lofgren DLL, the "output driver circuitry" is met by Fig. 2 of Redwine (e.g., NOR gate 76), and NOR gate 76 outputs data in response to the "internal clock signal" Φ1 as disclosed in Redwine Fig. 2. *See* Mot. at 11-12.

Rambus, in turn, also relies on its previous arguments for claim 35 of the '020 patent in arguing that claim 36 is not invalid as a matter of law. Opp. at 11 (citing Murphy Decl. ¶¶ 53-58). For the reasons discussed above, Hynix's motion for summary judgment of invalidity on claim 36 of the '020 patent is denied.

C. Asserted Claim 34 of the '105 Patent

Hynix contends claim 34 of the '105 patent, a claim that is dependent on claim 31, is invalid as obvious under 35 U.S.C. § 103.

1. Claim 31 of the '105 Patent

a. "A synchronous memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises"

The court construed "synchronous memory device" as "a memory device that receives an external clock signal which governs the timing of the response to a transaction request." Although the parties disagree over whether the Redwine patent discloses an "external clock signal," *see, e.g.*, Murphy Decl. ¶ 60, as discussed above, the court has concluded that Redwine discloses an "external clock signal."

b. "internal clock generation circuitry to generate a first internal clock signal and a second internal clock signal, wherein the internal clock generation circuit generates the first and second internal clock signals using at least a first external clock;"

Hynix relies on the top left hand corner of Fig. 3 of the Redwine reference as internal clock generation circuitry, identifying Φ as the external clock signal upon which the internal clock generation circuitry generates first and second internal clocks Φ1 and Φ2.

Rambus again counters that Φ is not an external clock signal because it is not periodic, and also that Φ is not shown as an input to the "clock generator and control" block of Fig. 1. *See* Murphy Decl. ¶¶ 61-62. As discussed above, the court has found that Redwine discloses an "external clock signal."

c. "an output driver, coupled to the internal clock generation circuitry, the output driver outputs data on a bus in response to the first and second internal clock signals and synchronously with respect to at least the first external clock signal"

Hynix again contends that "an output driver" is disclosed in Redwine Fig. 1 block 26, with a

more detailed description at Fig. 3. Specifically, in block 26 Hynix argues that NOR gate 75 outputs information to the memory device. Hynix then argues that the Fig. 3 of Redwine shows a multiplexer made up of transistors 72a, 72b, 74a, 74b and coupled between shift registers 20a, 20b and NOR gate 75. Redwine Patent Fig. 3; Redwine Chart at 1. The multiplexer is controlled by internal clock signals Φ1 and Φ2. *See* Redwine Patent Fig. 3, c.7, l:7-16. Thus, in a read operation, data is transferred from the shift registers to NOR gate 75 through the multiplexer under the control of internal clock signals Φ1 and Φ2, which are generated by at least the external clock signal Φ. Because NOR gate 75 outputs data in response to Φ1 and Φ2, and Φ1 and Φ2 have a known timing relationship with Φ, Hynix argues that NOR gate 75 outputs data synchronously with respect to the external clock signal Φ.

Rambus counters that a person of ordinary skill in the art, looking at Fig. 1 of the Redwine patent, would conclude that Φ is not shown as an input to the "clock generator and control" block of Fig. 1, and again argues that Φ is not an "external clock signal." *See* Murphy Decl. ¶¶ 63-64. The court is satisfied that the Redwine patent meets this limitation.

2. Underlying Question of Fact on Obviousness of Claim 34 of the '105 Patent

Claim 34 recites: "The memory device of claim 31 further including clock receiver circuitry to receive the first external clock and wherein the internal clock generation circuitry includes delay locked loop circuitry, coupled to the clock receiver circuitry, to generate the first internal clock signal and the second internal clock signal using at least the first external clock." In addition to the arguments discussed above, Hynix argues that Redwine discloses the use of two one-stage delay elements to generate delayed versions (Φ1d and Φ2d) of clock signals Φ1 and Φ2. *See* Redwine Patent Fig. 3, c.4, l:59-64; c..5, l:55-57.

Based on these arguments, Hynix submits that as per claim 35 of the '020 patent, one of skill in the art would have understood to integrate the DLL/PLL of the Lofgren patent with the memory of Redwine to generate an internal clock signal from an external clock signal to reduce or eliminate skew, increase performance, minimize bus setup and hold times, or to optimize signal timings on or between chips. On-chip DLL/PLL Chart at 5-6. Thus, Hynix argues that claim 34 of the '105 patent

is rendered obvious in view of Lofgren and Redwine.

Rambus again counters that Lofgren teaches a PLL (with a delay line), not a DLL (with a variable delay line), and that Lofgren does not relate to "synchronous DRAMS." Murphy Decl. ¶ 68. Rambus also reemphasizes that Lofgren teaches external control of DRAMs, and therefore teaches away from implementing a DLL on a DRAM memory chip; that Lofgren only discusses "conventional" DRAMs based on signal transitions of /RAS and /CAS signals; and that Φ is not a periodic signal. In addition, Rambus again notes the lack of evidence presented by Hynix on the non-obviousness factors, and points to materials relating to long-felt need, unsuccessful attempts by others, acceptance by others as shown by licensing agreements, and the lack of independent invention by others. *See id.* ¶¶ 69-71. For the reasons discussed above, the court finds that Hynix has failed to establish invalidity as a matter of law of claim 34 by combining the Redwine and Lofgren patents. *See In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000).

III. ORDER

For the foregoing reasons, the court DENIES Hynix's motion for summary judgment on each claim.

DATED: 2/28/06

/s/ Ronald M. Whyte
RONALD M. WHYTE
United States District Judge

THIS SHALL CERTIFY THAT A COPY OF THIS ORDER WAS PROVIDED TO:

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